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# Analysis and Mitigation of Flip-Flop Timing in Subthreshold Logic Design using Adaptive Feedback Equalization

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**Abstract:** Ultralow-power subthreshold logic circuit is becoming prominent in embedded application with the limited energy budget. Minimum energy consumption of digital logic circuits can be obtained by operating in subthreshold regime. However in this regime process variation can result in up to an order of magnitude variation in ION/IOFF ratios leading to timing errors, which can have a destructive effect on functionality of subthreshold circuits. This timing error become more frequent in scaled technology node where process variation are highly prevalent. Therefore, mechanism to mitigate these timing errors while minimizing the energy consumption are not required. We propose tunable adaptive feedback equaliser circuit that can be used along with a sequential digital logic circuit to mitigate proceed variation and reduce the dominant leakage energy.

**Keywords:** feedback equalizer, leakage energy component, subthreshold.

## I. INTRODUCTION

Since 1970's VLSI plays a major role in communication and semiconductor devices. VLSI (Very Large Scale Integration) comprises thousands of transistors on a single IC Chips. VLSI is majorly linked with Low power, Area and Speed. The Power Consumption is important phenomenon in many applications. VLSI. The use of subthreshold digital CMOS logic circuits is becoming increasingly popular in energy-constrained applications where high performance is not required. The main idea here is that scaling down the supply voltage can significantly reduce the dynamic energy consumed by digital circuits. Scaling the supply voltage also lowers down the leakage current due to reduction in the drain-induced barrier lowering (DIBL) effect. However, as the supply voltage is scaled below the threshold voltage of the transistors, the propagation delay of the logic gates increases, which in turn increases the leakage energy of the transistors. These two opposite trends in the leakage and the dynamic energy components lead to a minimum energy supply voltage that occurs below the threshold voltage of the transistors for digital logic circuits [1]. However, digital logic circuits operating in the subthreshold region suffer from process variations that directly affect the threshold voltage (VT). This in turn has a significant impact on the drive current due to the exponential relationship between the drive current and the threshold voltage of the transistors in the subthreshold regime. Moreover, subthreshold digital circuits suffer from the degraded ION/IOFF ratios [2] resulting in a failure in providing rail-to-rail output swings when restricted by aggressive timing constraints. These degraded ION/IOFF ratios and process-related variations make subthreshold circuits highly susceptible to timing errors that can further lead to complete system failures. Since the standard deviation of VT varies inversely with the square root of the channel area [3], one approach to overcome the process variation is to upsize the transistors [2]. Alternately, one can increase the logic path depth to leverage the statistical averaging of the delay across gates [4] to overcome process variations. These approaches, however, increase the transistor parasitics, which in turn increases the energy consumption. In this paper, we first propose the use of a feedback equalizer circuit for lowering the energy consumption of digital logic operating in the subthreshold region while achieving robustness equivalent to that provided by [2]. Here, the feedback equalizer circuit (placed just before the flip-flop) adjusts the switching threshold of its inverter based on the output of the flip-flop in the previous cycle to reduce the charging/discharging time of the flip-flop's input capacitance. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block. Overall, this reduces the total delay of the sequential logic, which makes it more robust to timing errors and allows aggressive clocking to reduce the dominant leakage energy. In addition to reducing energy consumption, we also demonstrate how the tuning capability of the equalizer can be used to enable extra charging/discharging paths for the flip-flop input capacitance after fabrication to mitigate timing errors resulting from worse than expected process variations in the subthreshold digital logic. In general, our approach of using feedback equalizer to lower energy consumption and improve robustness is

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independent of the methodology used for designing a combinational logic block operating in the subthreshold regime. The main contributions of this paper are as follows.

1) We propose using an adaptive feedback equalizer circuit in the design of tunable subthreshold digital logic circuits. This adaptive feedback equalizer circuit can reduce energy consumption and improve performance of the subthreshold digital logic circuits. At the same time, the tunability of this feedback equalizer circuit. enables post fabrication tuning of the digital logic block to overcome worse than expected process variations as well as lower energy and improve performance.

2) We present detailed analytical models (AMs) for performance and energy of the adaptive feedback equalizer circuit. These models can be easily used in combination with the existing performance and energy models for subthreshold circuits to generate subthreshold designs that meet energy and/or performance constraints.

The rest of this paper is organized as follows. Section II discusses the related work in the design of low-power robust subthreshold circuits. A detailed description of the operation of the adaptive feedback equalizer circuit in subthreshold regime is presented in Section 1. In Section 2, we explore the use of the adaptive feedback equalizer circuit in various digital logic circuits to improve energy efficiency and mitigate process variation effects.

## II. RELATED WORK

Several techniques have been proposed to design robust ultralow power subthreshold circuits. As described earlier, transistor upsizing [2] and increasing the logic path depth [4], [5] can be used to overcome process variations. The use of gates of different drive strengths has also been proposed to overcome process variations [6]. A detailed analysis on the timing variability and the metastability of the flip-flops designed in the subthreshold region has been presented in [7] and [8], respectively. Lotze and Manoli [9] have used the Schmitt trigger structures insubthreshold logic circuits to improve the ION/IOFF ratio and effectively reduce the leakage from the gate output node. Pu et al. [10] proposed a design technique that uses a configurable VT balancer to mitigate the VT mismatch of transistors operating in subthreshold regime. Zhou et al. [11] propose to boost the drain current of the transistors using minimum-sized devices with fingers to mitigate the inverse narrow width effect in subthreshold domain. An analytical framework for subthreshold logic gate sizing based on statistical variations has been proposed in [12], which provides narrower delay distributions compared with the state-of-the-art approaches. Body-biasing has also been proposed to mitigate the impact of variations [13].

A controller that uses a sensor to first quantify the effect of process variations on subthreshold circuits and then generates an appropriate supply voltage to overcome that effect has been proposed in [14]. De Vita and Iannaccone [15] have used a current reference circuit to design a voltage regulator. providing a supply voltage that makes the propagation delay of the subthreshold digital circuits almost insensitive to temperature and process variations. Using a differential dynamic logic in standby mode, Liu and Rabaey propose to suppress leakage in the subthreshold circuits. Error detection and correction techniques have been widely used to design resilient, energy-efficient abovethreshold architectures. Tschanz et al and Bowman and Tschanz have used a tunable replica circuit (with 3.5% leakage power overhead, 2.2% area overhead), and error-detection sequentials (with 5.1% leakage power overhead and 3.8% area overhead) to monitor critical path delays and mitigate dynamic variation guardbands for maximum throughput in the above-threshold regime. Using an adaptive clock controller based on error statistics, the proposed processor architecture operates at maximum efficiency across a range of dynamic variations. Bull et al. applied Razor error correction technique (with 9.4% power overhead and 6.9% areaoverhead) to a 32-bit ARM processor with a microarchitecture design for energy-efficient operation through the elimination of timing margins. Whatmough et al. applied Razor (with 16.9% power overhead and 1.59% area overhead) to a 16-tap finite-impulse response (FIR) filter realizing a 37% improvement in energy efficiency.

These error correction techniques could be potentially used in combination with our feedback equalization technique to improve robustness in sequential logic blocks operating in the subthreshold regime. We propose a circuit-level scheme that uses a communication-inspired feedback equalization technique in the critical path to mitigate the timing errors rising from aggressive voltage scaling and process variations in subthreshold digital logic circuits. It should be noted that we are not designing subthreshold communication circuits. We are proposing the design of subthreshold logic circuits that leverage principles of communication theory. Several authors have already used feedback-based techniques to boost the weak low-voltage signals in global interconnections Seo et al. proposed the self-timed regenerator technique to improve the speed and power for on-chip global interconnects leading to 14% delay improvement over the conventional repeater design in the above-threshold regime. Schinkel et al. presented a pulse width preemphasis equalization approach with lower latency compared with the classic repeater insertion technique. Kim and Seok proposed a reconfigurable interconnect design technique based on regenerators for ultradynamic voltage- scaling systems to improve performance and energy efficiency across a large range of above-threshold supply voltages. Seo et al. proposed the design of an adaptively controlled preemphasis transceiver to reduce intersymbol interference in on-chip signaling. Kim and Stojanovi´c presented an energy-efficient transceiver design that performs Feedforward equalization for repeaterless, high-performance on-chip communication. Equalization techniques have been proposed to design energy-efficient logic circuits operating in the above-threshold regime.

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Takhirov et al. proposed to use the feedback equalizer circuit with Schmitt trigger to mitigate timing error
Equalization techniques have been proposed to design energy-efficient logic circuits operating in the above-threshold regime. Takhirov et al. proposed to use the feedback equalizer circuit with Schmitt trigger to mitigate timing errors resulting from voltage scaling and in turn improve energy efficiency for the above-threshold logic circuits. Similarly, Zangeneh and Joshi [28] used feedback equalization to reduce the dominant leakage energy of subthreshold logic circuits. However, this technique is static and it does not have the capability to handle worse than expected intradie and interdie process variations. We propose using an adaptive feedback equalizer circuit in the design of tunable subthreshold digital logic circuits. This adaptive feedback equalizer circuit can reduce energy consumption and improve performance of the subthreshold digital logic circuits. Moreover, the tunability of this feedback equalizer circuit enables post fabrication tuning of the digital logic circuit to overcome worse than expected process variations as well as improve energy and performance. the input signals change.

## ADAPTIVE EQUALIZED FLIP-FLOP VERSUS CONVENTIONAL FLIP-FLOP

In this section, we first explain the use of the adaptive feedback equalizer circuit in the design of an adaptive equalized flip-flop (E-flip-flop) and then provide a detailed comparison of the E-flip-flop with the conventional flip-flopin terms of area, setup time, and performance. We propose theuse of a variable threshold inverter [26] (Fig. 1) as an adaptive feedback equalizer along with the classic master–slave positive edge-triggered flip-flop [29] (Fig. 2) to design an adaptive E-flip-flop. This adaptive feedback equalizer circuit consists of two feedforward transistors (M1 and M2 in Fig. 1) and four control transistors (M3 and M4 for feedback path 1 that is always ON and M5 and M6 for feedback path 2 that can be conditionally switched ON postfabrication in Fig. 1) that provide extra pull-up/pull-down paths in addition to the pull-up/pull-down path in the static inverter for the Data Flip-Flop input capacitance. The extra pull-up/pull-down paths areenabled whenever the output of the critical path in the combinational logic changes. The control transistors M5 and M6are enabled/disabled through transistor switches (M7 and M8) that are controlled by an asynchronous control latch. The value of the static control latch is initially reset to 0 during chip bootup. After bootup, if required a square pulse is sent to the En terminal to set the output of the latch to 1 to switch ON M7 and M8, which enables feedback path 2. The adaptive E-flip-flop effectively modifies the switching threshold of the static inverter in the feedback equalizer based on the output of flip-flop in the previous cycle. If the previous output of the flip-flop is a 0, the switching threshold of the static inverter is lowered, which speeds up the transition of the flip-flop input from 0 to 1. Similarly if the previous output is 1, the switching threshold is increased, which speeds up the transition to 0. Effectively, the circuit adjusts the switching threshold and facilitates faster high-to-low and low-to-high transitions of the flip-flop input. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block. Overall, this reduces the total delay of the sequential logic. The dc response of the adaptive feedback equalizer circuit with two different feedback paths in the subthreshold regime is shown in Fig. 3. The adaptive E-flip-flop has eight more transistors than the conventional master–slave flip-flop [29]. Compared with a classic master–slave flip-flop with 22 transistors [seven inverters and four transmission gates (TGs)], the area overhead of the adaptive E-flip-flop is 36%. The area overhead of the control latch with ten transistors (three inverters and two TGs)is 45%. This area overhead gets amortized across the entire sequential logic block.

### Existing system

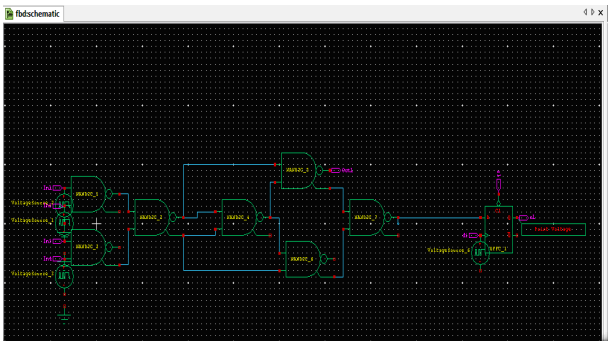
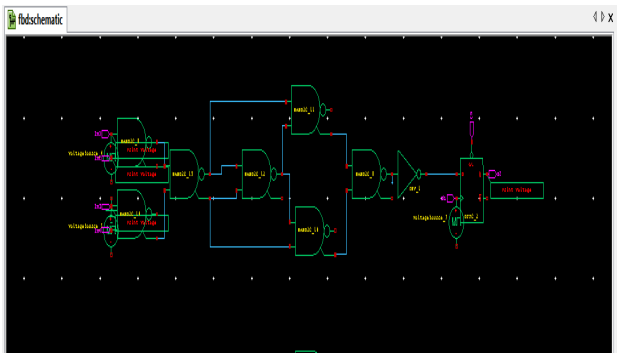
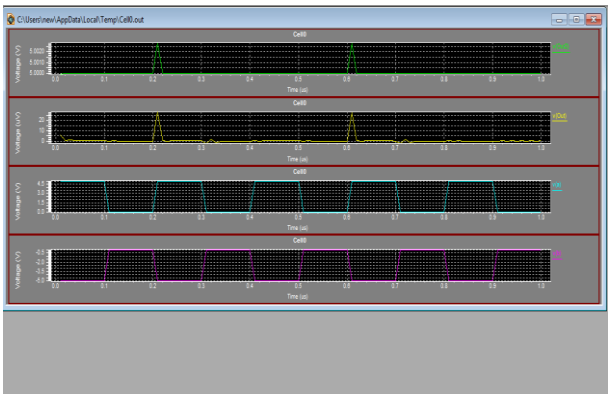


**Fig (1) non equallised flip-flop equalizer circuit**



**Fig(2) buffer inserted flip-flop**



**Fig(3) output wave form an existing system**

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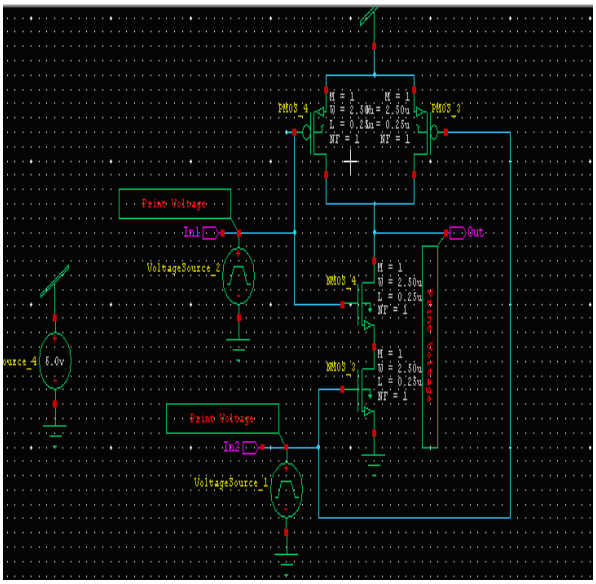
EXISTING SYSTEM

In this system combinational circuit whose output is directly given to flip-flop input it consume more power and it does not have feedback circuits. This is upsized to account for the process variation effects based on design methodology proposed. Using a minimum sized inverter instead of an upsized inverter would further lower down the delay but has low reliability with respect to the dominant process variation in subthreshold region

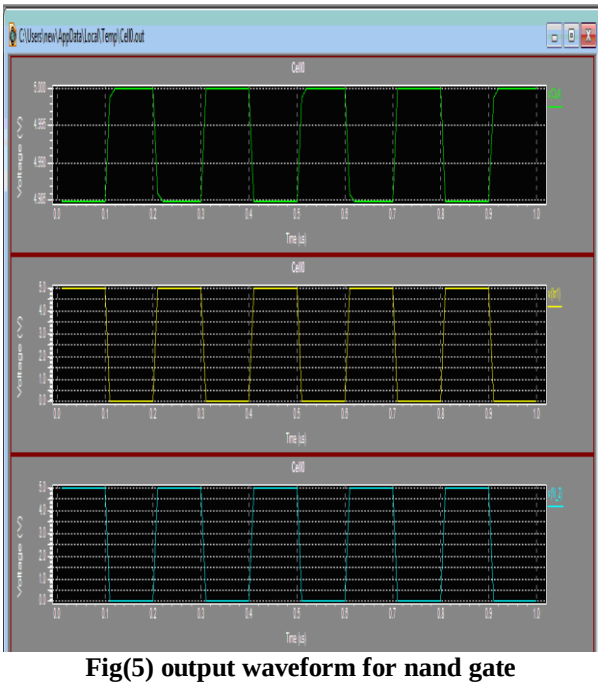
## III. PROPOSED ARCHITECTURE

ADAPTIVE E FLIP-FLOP



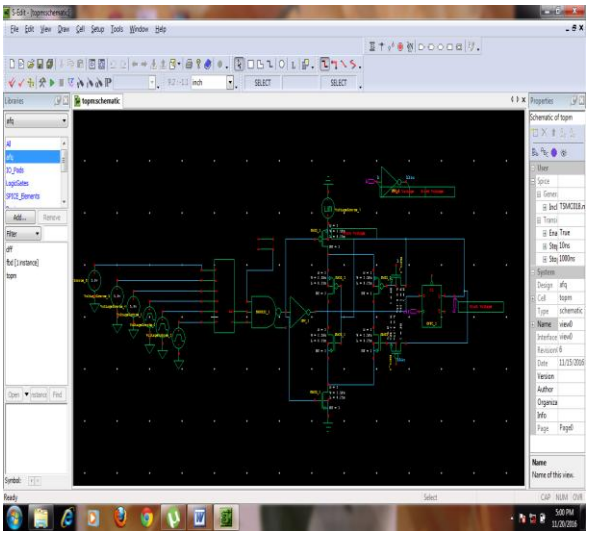

**Fig(4) Schematic diagram for nand gate**

OUTPUT WAVEFORMS



**Fig(5) output waveform for nand gate**

STRUCTURE OF ADAPTIVE E FLIP-FLOP



**FIG(6) ADAPTIVE E-FLIPFLOP**

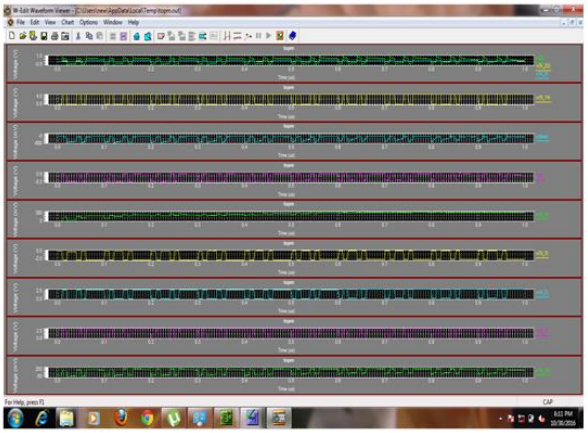


**Fig (7) shows output of adaptive Eflip-flop**

## IV. CONCLUSION

We proposed the application of a tunable adaptive feedback equalizer circuit to reduce the normalized variation of total delay along the critical path and the dominant leakage energy of the digital CMOS logic operating in the subthreshold regime. Adjusting the switching thresholds of the gates before flip-flop based on the gate output in the previous cycle, the adaptive feedback equalizer circuit enables a faster switching of the gate outputs and provides the opportunity to reduce the leakage energy of digital logic in weak inversion region.

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